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IN THE CLAIMS

Please cancel claims 38, 42-50, and 53.

Please amend claims 35 and 63.

1-34. (Cancelled)

35. (Currently amended) A method of fabricating at least one inverter comprising:

providing a semiconductor of a first type conductivity;

forming a well of a second type conductivity in the semiconductor;

forming a first type transistor in the well, wherein the first type transistor has a first source, a first drain, and a first gate;

forming a first contact in the well in spaced relation to the first type transistor;

forming a second contact in the well in spaced relation to the first type transistor;

coupling the first contact to a first voltage input; and

coupling the second contact to the first source, wherein the first source is coupled to the first voltage input through a parasitic resistance of the well.

36. (Previously presented) The method of claim 35, wherein forming a first contact comprises forming a first contact a first distance from the first source, wherein the first distance defines a first component of a parasitic resistance of the well; and

wherein forming a second contact comprises forming a second contact a second distance from the first source, wherein the second distance defines a second component of the parasitic resistance of the well.

37. (Previously presented) The method of claim 35 wherein:

forming a well comprises forming an n-type well in the semiconductor;

forming a first type transistor comprises forming a first p-type region in the well defining the first source, forming a second p-type region in the well defining the first drain and forming the first gate over the well.

38-50. (Cancelled)

51. (Previously presented) The method of claim 35 wherein coupling the first source to the second contact comprises forming an interconnect layer over the semiconductor.

52. (Previously presented) The method of claim 51 wherein the interconnect layer comprises a metallization connection.

53. (Cancelled)

54. (Previously presented) The method of claim 36 wherein the the first source is coupled to the first voltage input through the series combination of the first and second components of the parasitic resistance of the well.

55. (Previously presented) The method of claim 36 wherein the first and second contacts are positioned in the well such that the distance from the first contact to the second contact is greater than the distance from the first contact to the first source.

56. (Previously presented) The method of claim 35, wherein the first type transistor is positioned between the first and second contacts.

57. (Previously presented) The method of claim 35 further comprising forming a plurality of first type transistors in the well, each of the first type transistors having a source coupled to the second contact.

58. (Previously presented) The method of claim 35 further comprising:

forming a second type transistor in the substrate outside of the well;

coupling the second type transistor to a second voltage input; and

coupling the semiconductor to a third voltage input proximate to the second type transistor.

59. (Previously presented) The method of claim 58 wherein the third voltage input comprises a substrate tie down contact.

60. (Previously presented) The method of claim 58 wherein the first type transistor comprises a pull up transistor, and wherein the second type transistor comprises a pull down transistor.

61. (Previously presented) The method of claim 58, further comprising:

forming a plurality of first type transistors formed in the well, each of the first type transistors having a source, a drain, and a gate, wherein the source of each first type transistor is coupled to the second contact;

forming a plurality of second type transistors in the substrate outside of the well; and,

coupling each of the plurality of second type transistors to a second voltage input.

62. (Previously presented) The method of claim 61, wherein each of the plurality of second type transistors has a source, a drain, and a gate, wherein each gate of the plurality of second type transistors is coupled to the gate of an associated one of the plurality of first type transistors in the well, each source of the plurality of second type transistors is coupled to the second voltage input, and each drain of the plurality of second type transistors is coupled to the drain of an associates one of the plurality of first type transistors in the well.

63. (Currently amended) A method of fabricating at least a first inverter comprising:

providing a semiconductor of a first type conductivity;

forming a well of a second type conductivity in the semiconductor;

forming a first type transistor in the well, wherein the first type transistor has a first source, a first drain, and a first gate;

forming a first contact in the well in spaced relation to the first type transistor;

forming a second contact in the well in spaced relation to the first type transistor;

coupling the first contact to a first voltage input; and

coupling the second contact to the first source through a connection from the well over the semiconductor, wherein the first source is coupled to the first voltage input through a parasitic resistance of the well.